

Claim Amendments

1-10. (canceled)

11. (previously presented) An input protection circuit comprising:
a voltage supply node and a ground node;
an MOS circuit coupled to the voltage supply node and to the ground
node;

a transistor coupled to the voltage supply node and to the ground node in
parallel with the MOS circuit and having a first junction region coupled to the
voltage supply node, a second junction region coupled to the ground node, a
junction-free substrate region between the first and second junction regions, an
MOS gate electrode overlying the substrate region and separated therefrom by a
gate oxide layer, and dielectric sidewall spacers adjacent to opposing sides of
the MOS gate electrode and overlying the junction-free substrate region;

a compensating diode coupled to the voltage supply node and to the
ground node in parallel with the MOS circuit and the transistor; and

wherein the second junction region and the substrate region comprise a
semiconductor material of the same conductivity type.

12. (previously presented) The input protection circuit of claim 11 wherein the
transistor comprises a plurality of 1 to N forward biased diodes connected in
series, such that the first junction region of the first diode is coupled to the
voltage supply node and the second junction region of the Nth diode is coupled
to the ground node.

13-21. (canceled)

26. (new) A circuit comprising:

an MOS circuit coupled to a voltage supply node and a ground node;
a lateral high-voltage junction device for over voltage protection of the
MOS circuit, the device coupled to the voltage supply and ground node in parallel
with the MOS circuit; and
a compensating diode coupled to the voltage supply and ground node in
parallel with the MOS circuit and the lateral high-voltage junction device.

22. (currently amended) A circuit comprising:
an MOS circuit coupled to a voltage supply node and a ground node; and
a lateral high-voltage junction device for over voltage protection of the
MOS circuit, the device coupled to the voltage supply and ground node in parallel
with the MOS circuit, the device comprising:

a substrate having a first junction region separated from a second
junction region by a uniformly doped substrate region extending from the
first junction region to the second junction region;

an MOS gate electrode overlying the uniformly doped substrate
region and separated therefrom by a gate oxide layer; and

dielectric sidewall spacers adjacent to opposing sides of the MOS
gate electrode and overlying the uniformly doped substrate region; and
a compensating diode coupled to the voltage supply and ground node in
parallel with the MOS circuit and the lateral high-voltage junction device.

23. (canceled)

24. (previously presented) The circuit of claim 22, wherein the first junction
region and the substrate region comprise semiconductor materials of different
conductivity types, the first junction being coupled to the voltage supply node,
and the second junction and the substrate region comprise a semiconductor
material of the same conductivity types, the second junction being coupled to the
ground node.

25. (previously presented) The circuit of claim 22, wherein the first junction
region comprises an anode and the second junction region comprises a cathode,
and wherein the anode and the cathode have an opposite conductivity type.